

JAYDEN KOH

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👤 **Citizenship:** U.S. Citizen

EDUCATION

Texas A&M University

Expected Graduation: 12/27

Bachelor of Science in Computer Engineering, Minor in Mathematics, Minor in Cybersecurity

GPA: 3.82

RELEVANT COURSEWORK

Computer Architecture, Operating Systems, Embedded Systems, Microprocessor Design, Advanced Digital Systems Design, Parallel Computing, Data Structures & Algorithms, Probability & Statistics, Linear Algebra

SKILLS

Hardware & Verification: SystemVerilog, SVA, Verilog, Formal Verification, RTL Simulation, CPU/SoC Verification, Coverage-Guided Verification, FPGA, Vivado, Synopsys VCS, Verilator, Chipyard

Computer Architecture: RISC-V, CPU Microarchitecture, SoC Architecture, Privilege Modes, ISA-Level Debugging, Architectural Traces, Hardware/Software Co-Design

Languages & Tools: C, C++23, Python, Bash/Shell, Linux, Git, Docker, CMake/Make

Low-Level Systems: Bare-Metal Firmware, Bootloaders, Linker Scripts, Memory Maps, MMIO, Interrupts, JTAG, ILA, GDB

PROJECTS

FPGA Real-Time Telemetry & Hardware Diagnostics

- Built a synthesizable FPGA data-processing pipeline with FIFO-based burst handling, clock-domain crossing, latency profiling, and UART/JTAG instrumentation operating at **200 MHz**.
- Implemented cycle-level latency measurement and event tracing, closing timing at **+0.8 ns WNS** on an Artix-7 FPGA.

Rev Silicon Formal Verification

- Designed **SystemVerilog Assertions** for AI accelerator modules including matrix multiplication FSMs, arbiters, and FIFOs.
- Developed formal **assertion, assumption, and cover properties** to verify safety, liveness, and fairness requirements during pre-silicon RTL verification.

EXPERIENCE

Sandia National Lab

May 2026 – Present

Cybersecurity Intern (RISC-V SoC Design & Bring-Up)

Livermore, California

- Designed and brought up a **RISC-V SoC** around **PicoRV32**, integrating ROM, RAM, UART, GPIO, and memory-mapped peripherals through a unified address space for simulation and FPGA deployment.
- Redesigned the memory subsystem from combinational storage to **synchronous BRAM-compatible interfaces**, implementing ready/valid handshaking and debugging instruction/data transaction issues across the shared processor bus.
- Developed **SystemVerilog testbenches** and bare-metal RISC-V firmware to validate processor, memory, and MMIO behavior, using architectural state, waveform analysis, and UART telemetry to isolate **hardware/software integration failures**.

Secure and Trustworthy Hardware Lab

Aug 2024 – December 2025

RISC-V Simulation & Verification Researcher

College Station, Texas

- Built a Python-based RISC-V RTL verification framework integrating randomized instruction generation, RTL simulation, coverage collection, Spike golden-model comparison, failing-seed replay, and architectural mismatch triage.
- Integrated and brought up Rocket, BOOM, CVA6/CVA6S, RSD, and Ibex targets, debugging boot flow, memory maps, linker behavior, privilege-mode transitions, and hardware/software interface failures.
- Improved experimental coverage by 2x over prior work and uncovered six previously unknown privilege-escalation vulnerabilities through coverage-guided testing and hardware fuzzing.
- Led six undergraduate researchers across processor integration, coverage objectives, regression debugging, failure reproduction, and architectural trace analysis.

Lockheed Martin

Jan 2026 – May 2026

Software Engineering Intern - Embedded Systems

Owego, New York

- Validated multistage boot sequences, hardware discovery, device interfaces, and system bring-up using requirements-based testing, GDB, system logs, and hardware-level investigation.

MIT Lincoln Lab

May 2023 – Aug 2024

Associate Instructor, Embedded Security

Boston, Massachusetts

- Designed and implemented a secure remote firmware update system for resource-constrained ARM Cortex-M microcontrollers.
- Implemented signed manifest validation, authenticated firmware updates, rollback prevention, and secure boot verification.